REMARKS

This Amendment responds to the Office Action mailed July 17, 2007 in the above-identified application. Based on the foregoing amendments and the following comments, reconsideration and allowance of the application are respectfully requested.

Claims 1-3, 5-8, 11-15, 17-19 and 22-30 were previously pending in the application. By this Amendment, claims 2, 5, 11, 18, 19, 22, 25 and 29 have been amended. Claims 1, 3, 15, 17 and 26 have been canceled without prejudice or disclaimer. New claims 31-35 have been added. Claims 1 and 17 have been rewritten as new claims 31 and 34, respectively. Accordingly, claims 2, 5-8, 11-14, 18, 19, 22-25 and 27-35 are currently pending, with claims 31 and 34 being independent claims. The new claims find clear support in the original application at least at FIGs. 3 and 6; page 8, line 26 to page 9, line 9; page 15, lines 9-19; and page 17, line 15 to page 18, line 2. No new matter has been added.

The Examiner has rejected claims 1-3, 5-8, 11-15, 17-19 and 22-30 under 35 U.S.C. §102(b) as anticipated by Parthasarathy (US 6,617,799). The rejection is respectfully traversed in view of the amended claims.

Parthasarathy discloses a system and method for dynamically sizing hardware loops and executing nested loops in a digital signal processor. The disclosed apparatus includes N pairs of loop start registers and loop end registers, each loop start register storing a loop start address and each loop end register storing a loop end address, and N comparators, each of the N comparators associated with one of the N pairs of loop start registers and loop end registers. Each of the N comparators compares a selected one of a first loop start address and a first loop end address to a fetch program counter to detect one of the loop start hit and a loop end hit (col. 2, lines 14-25). The fetch stage compares the fetch PC value to the contents of all three loop addresses corresponding to the three loops (col. 5, lines 31-33). The loop start/end detection circuit is shown in FIG. 3 of Parthasarathy. Output results of comparators 321-323 are provided to priority match circuitry 305, which resolves instances of multiple hits according to the convention that loops are always fully nested (col. 7, lines 31-38).

Regarding new claim 31, Parthasarathy does not disclose or suggest a method for issuing instructions in a processor having pipeline, comprising, in part, *(d) issuing loop instructions corresponding to the first loop setup instruction speculatively after the loop control parameters are written in the current entry in the register file and before the first loop setup instruction has completed execution in the pipeline, wherein the current entry in the register file contains speculative copies of the loop control parameters, and (e) marking the current entry in the register file as an architectural entry when the first loop setup instruction has completed execution in the pipeline,* as required by claim 31. Parthasarathy contains no disclosure or suggestion of issuing loop instructions speculatively before the loop setup instruction has completed execution in the pipeline or of marking the current entry in the register file as an architectural entry when the first loop setup instruction has completed execution in the pipeline. Furthermore, Parthasarathy contains no disclosure whatever of a method for setting up a hardware loop wherein loop instructions are issued speculatively. For at least these reasons, new claim 31 is clearly and patentably distinguished over Parthasarathy.

Claims 2, 5-8, 11-14, 32 and 33 depend from claim 31 and are patentable over Parthasarathy for at least the same reasons as claim 31.

Regarding new claim 34, Parthasarathy does not disclose or suggest apparatus for issuing instructions in a processor having a pipeline, comprising, in part, a controller including *means for issuing loop instructions corresponding to the first loop setup instruction speculatively after the loop control parameters are written in the current entry in the register file and before the first loop setup instruction has completed execution in the pipeline, wherein the current entry in the register file contains speculative copies of the loop control parameters, and means for marking the current entry in the register file as an architectural entry when the first loop setup instruction has completed execution in the pipeline,* as required by claim 34. As indicated above, Parthasarathy contains no disclosure or suggestion of issuing loop instructions speculatively before the loop setup instruction has completed execution in the pipeline or of marking the current entry in the register file as an architectural entry when the first loop setup instruction has completed execution in the pipeline. Furthermore, Parthasarathy contains no disclosure

whatever of a method for setting up a hardware loop wherein loop instructions are issued speculatively. For at least these reasons and for the reasons discussed above in connection with claim 31, new claim 34 is clearly and patentably distinguished over Parthasarathy.

Claims 18, 19, 22-25, 27-30 and 35 depend from claim 34 and are patentable over Parthasarathy for at least the same reasons as claim 34.

Based upon the above discussion, claims 2, 5-8, 11-14, 18, 19, 22-25 and 27-35 are in condition for allowance.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Dated: December 14, 2007

Respectfully submitted,

By William R. McClellan

William R. McClellan
Registration No.: 29,409
WOLF, GREENFIELD & SACKS, P.C.
Federal Reserve Plaza
600 Atlantic Avenue
Boston, Massachusetts 02210-2206
(617) 646-8000

X12/17/2007